## REMARKS/ARGUMENT

**Regarding the Amendments to the Specification:**

Several minor errors noted in the specification during preparation of this response have been corrected. No new matter has been introduced.

**Regarding the Claims in General:**

Claims 5-9, 11-13, and 15-18 are now pending. Claim 4 has been rewritten in independent form as new claim 15, and claims 1, 3, and 4 have been canceled without prejudice. Claims 5 and 6 have been amended, and are also now in independent form. Claims 2, 10, and 14 have also been canceled without prejudice. Claim 7, previously incorrectly dependent on claim 1 is now dependent on claim 5. Claim 12, previously incorrectly dependent on claim 10 has been corrected, and is now dependent on claim 11.

New claims 16-22 have been added to provide applicant with additional protection to which he appears to be entitled in light of the known prior art.

**Regarding the Prior Art Rejections:**

In the outstanding Office Action, claims 1-14 were rejected as anticipated by Lesea U.S. Patent 5,315,214 (Lesea). Applicant respectfully submits that this rejections is not applicable to the claims now pending. Reconsideration and withdrawal of the rejection are accordingly requested.

All of the pending claims focus on features of the power factor correction aspect of the invention. New claim 15 (which has been substituted for claim 4) and new claims 20-22, for example, call for power factor correction circuitry which:

> . . . includes a boost type power converter operated in critical conduction mode.

Claim 5, as amended, and new claims 18 and 19 specify that the power factor control circuitry:

> . . . is selectively operable at a high gain to obtain a fast response or at a low gain for power factor correction optimization.

Claim 6, as amended, and new claims 16 and 17 specify that the power factor control circuitry:

> . . . includes a switch, an on time of the switch being increased when a voltage of the input power approaches zero.

None of these features are found in Lesea, so far as can be determined.

Method claim 8 calls for:

> sensing a zero crossing of an input voltage;
>
> increasing a switch on time as the input voltage approaches the zero crossing to provide for power factor correction with reduced crossover distortion;
>
> increasing a gain of a power factor correction loop to obtain a fast response;
>
> reducing a gain of a power factor correction loop to optimize ballast power factor; and
>
> controlling an inductor by activating a switch in a boost type power factor correction circuit.

This combination of features is also not disclosed, taught or suggested by Lesea.

Claim 11 is directed to a power factor correction circuit integrated into an electronic ballast. The features of this claim not disclosed, taught or suggested by Lesea include:

> . . . a variable gain control section coupled to the input voltage sensing section and operable to provide variable closed loop feedback gain in the power factor correction circuit;
>
> a compensation indication coupled to the variable gain control section for influencing a closed loop gain of the variable gain control section;
>
> an output section coupled to the variable gain control section . . . for driving a power factor correction switch, an on time of the output section being related to the input voltage, the variable closed loop gain and the zero current crossing.

As all the above-mentioned claims recite features not disclosed, taught or suggested in Lesea, these claims are not anticipated, and should be allowed.

Claim 9 is dependent on claim 8, and claims 12 and 13 are dependent on allowable claim 11. These claims also should be allowed for the reasons stated above. In addition, these claim recite

features which, in combination with the features of their respective parent claims are neither disclosed, taught nor suggested in Lesea.

In view of the foregoing, favorable reconsideration and allowance of this application are respectfully solicited.

I hereby certify that this correspondence is being transmitted by Facsimile to (703) 872-9306 addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date indicated below.

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March 21, 2005
Date of Signature

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Respectfully submitted,

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